Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT**
2. **SENSE**
3. **SHUTDOWN**
4. **GRD**
5. **N. ERROR**
6. **5V TAP**
7. **FEEDBACK**
8. **INPUT**

**4 3 2 1**

**5 6 7 8**

**NOTES: Chip back must be connected to GND.**

**This Chip looks the same as LP2950 except that the fuselink**

**Between pads 6 and 7 is open circuit in the case of the LP2951.**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0031” X .0031”**

**Backside Potential: GROUND**

**Mask Ref: LP20C**

**APPROVED BY: DK DIE SIZE .036” X .066” DATE: 3/3/17**

**MFG: NATIONAL THICKNESS .012” P/N: LP2951**

**DG 10.1.2**

#### Rev B, 7/19/02